UNITED STATES PATENT AND TRADEMARK OFFICE

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/776,735	02/06/2001	Todd P. Lukanc	50432-086	2371

		EXAMINER
7590	05/06/2005	LEVIN, NAUM B

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ART UNIT	PAPER NUMBER
2825	

DATE MAILED: 05/06/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

PTO-90C (Rev. 10/03)

	Application No.	Applicant(s)
Office Action Summary	09/776,735	LUKANC, TODD P.
	Examiner	**Art Unit**	
	Naum B. Levin	2825	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE _3_ MONTH(S) FROM
THE MAILING DATE OF THIS COMMUNICATION.
- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed
  after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
  Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any
  earned patent term adjustment. See 37 CFR 1.704(b).

Status

1) ☒ Responsive to communication(s) filed on _01 March 2005_.

2a) ☐ This action is **FINAL.**   2b) ☒ This action is non-final.

3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is
closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4) ☒ Claim(s) _1-4 and 6-15_ is/are pending in the application.

    4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5) ☒ Claim(s) _8-12 and 14_ is/are allowed.

6) ☒ Claim(s) _1-3,13 and 15_ is/are rejected.

7) ☒ Claim(s) _4,6 and 7_ is/are objected to.

8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9) ☐ The specification is objected to by the Examiner.

10) ☒ The drawing(s) filed on _06 February 2001_ is/are: a) ☒ accepted or b) ☐ objected to by the Examiner.

    Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

    Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

    a) ☐ All   b) ☐ Some * c) ☐ None of:

      1. ☐ Certified copies of the priority documents have been received.

      2. ☐ Certified copies of the priority documents have been received in Application No. _____.

      3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage
application from the International Bureau (PCT Rule 17.2(a)).

    * See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)

2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)

3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)
    Paper No(s)/Mail Date _____.

4) ☐ Interview Summary (PTO-413)
    Paper No(s)/Mail Date. _____ .

5) ☐ Notice of Informal Patent Application (PTO-152)

6) ☐ Other: _____.

DETAILED ACTION

This office action is in response to application 09/776,735 and amendment filed

on 03/01/2005. Claims 1-4 and 6-15 remain pending in the application.

Based on the Response Examiner has performed additional search, and found a

new reference.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all

obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 1-3, 13 and 15 are rejected under 35 U.S.C. 103(a) as being

unpatentable over Eden et al. (US Patent 5,620,916) in view of Kotani et al (US Patent

6,853,743).

1. <u>As to claims 1, 13 and 15</u> Eden discloses method for improving via/contact

coverage in an integrated circuit including:

(1), (15) A method/computer-readable medium bearing instructions for

generating a circuit layout comprising (col.3, ll.54-56):

selecting at least one via that has at least one edge touching

(covering/overlapping/contact area) an edge of an overlying metal line (col.4, ll.65-66;

col.5, ll.12-18);

measuring (CAD tool is generally used by designers to aid in generating the

initial layout, wherein all interconnect lines are spaced by at least minimum distance;

whereby CAD tool is measuring distance between metal lines) a distance between the edge of the overlying metal line and an edge of an adjacent metal line (col.4, ll.35-44; col.4, ll.58-64);

if the distance between the touched edge of the overlying metal line and the edge of the adjacent metal line is at least a predetermined distance (minimum distance), then increasing the dimension of the overlying metal line (col.4, ll.35-44; col.4, ll.66-67; col.5, ll.1-11);

(13) An apparatus (computer system) for generating circuit layouts comprising:

a central processing unit (col.1, ll.33-45);

a display (col.1, ll.33-45); and

at least an input device (col.1, ll.33-45); wherein

the central processing unit (col.1, ll.33-45):

selects at least one via that has at least one edge touching (covering/overlapping/contact area) an edge of an overlying metal (col.4, ll.65-66; col.5, ll.12-18);

measures (CAD tool is generally used by designers to aid in generating the initial layout, wherein all interconnect lines are spaced by at least minimum distance; whereby CAD tool is measuring distance between metal lines) a distance between the edge of the overlying metal line and an edge of an adjacent metal line (col.4, ll.35-44; col.4, ll.58-64);

if the distance between the touched edge of the overlying metal line and the edge of the adjacent metal line is at least a predetermined distance (minimum distance),

then increases the dimension of the overlying metal line (col.4, ll.35-44; col.4, ll.66-67; col.5, ll.1-11).

With respect to claims 1, 13 and 15 Eden teaches the features above but lacks a method/apparatus/program for generating a circuit layout in which if the distance between the touched edge of the overlying metal line (contact area) and the edge of the adjacent metal line is less than the predetermined distance (minimum distance), then increasing a dimension of the overlying metal line and decreasing a dimension of the adjacent metal line.

As to claims 1, 13 and 15 Kotani in view of Eden discloses:

A method/apparatus/computer-readable medium bearing instructions for generating a circuit layout comprising:

if the distance between the touched edge of the overlying metal line and the edge of the adjacent metal line is less than the predetermined distance, then increasing a dimension of the overlying metal line and decreasing a dimension of the adjacent metal line (Abstract; col.2, ll.48-67; col.3, ll.1-2; col.5, ll.47-67; col.6, ll.1-14).

It would have been obvious to a person of ordinary skills in the art at the time the invention was made to employ Kotani's teaching regarding the method/apparatus/program for generating a circuit layout in which if the distance between the touched edge of the overlying metal line (contact area) and the edge of the adjacent metal line is less than the predetermined distance (minimum distance), then increasing a dimension of the overlying metal line and decreasing a dimension of the

adjacent metal line and use it in Eden's invention to provide a circuit layout correction

method for realizing high-precision correction within a short correction time.

2. <u>As to claims 2 and 3</u> Eden in view of Kotani recites:

(2) The method according to claim 1, comprising increasing the dimension of the

overlying metal line (contact area) in a vicinity of the via line (col.4, II.35-44; col.4, II.66-

67; col.5, II.1-11);

(3) The method according to claim 2, comprising increasing the dimension of the

overlying metal line according to a 3 sigma via-to-metal dimension and positioning error

factor for the technology embodied in the computer generated circuit layout (col.4, II.11-

30; col.5, II.26-31).

Allowable Subject Matter

3. Claims 4 and 6-7 are objected to as being dependent upon a rejected base

claim, but would be allowable if rewritten in independent form including all of the

limitations of the base claim and any intervening claims.

The following is a statement of reasons for the indication of allowable subject

matter:

The prior art of record fails to teach or suggest or render obvious:

A method for generating a circuit layout comprising:

selecting at least one via that has at least one edge touching an edge of an

overlying metal measuring a distance between the edge of the overlying metal line and

an edge of an adjacent metal line;

if the distance between the touched edge of the overlying metal line and the edge

of the adjacent metal line is at least a predetermined distance, then increasing the

dimension of the overlying metal line; and

if the distance between the touched edge of the overlying metal line and the edge

of the adjacent metal line is less than the predetermined distance, then increasing a

dimension of the overlying metal line and decreasing a dimension of the adjacent metal

line, wherein

decreasing the dimension of the adjacent metal line by an amount that accounts

for the

predetermined distance and a distance delta that is determined from evaluation of

simulated and experimental measurements of a distance where one metal line does not

electrically impact an adjacent metal line; and

increasing the dimension of the overlying metal line by an amount based upon

evaluation of simulated and experimental measurements of a distance where one metal

line does not impact an adjacent metal line.

4. Claims 8-12 and 14 are allowed.

The following is a statement of reasons for the indication of allowable subject

matter:

The prior art of record fails to teach or suggest or render obvious:

A method/apparatus/program for generating a circuit layout comprising:

determining a delta distance based upon simulated and experimental

measurements of metal lines in the circuit layout such that a metal line reduced by at

least the delta distance will not electrically impact an adjacent metal line that is increased by a second oversize;

determining the second oversize based upon simulated and experimental measurements of metal lines in the circuit layout such that increasing a metal line by the second oversize will not electrically impact an adjacent metal line that has been decreased by at least the delta distance;

selecting vias that do not fully contact a metal line based upon whether at least one edge of a via touches an edge of an overlying metal line, and grouping the selected vias into a first via group;

selecting vias in the first via group based upon whether a distance from the overlying metal line edge to an edge of an adjacent metal line is at least the minimum distance, and grouping these selected vias into a second via group;

increasing the dimension of the overlying metal lines that contact vias in the second via group by the first oversize;

increasing the dimension of metal lines that contact vias in the first via group that are not in the second via group by the second oversize; and

decreasing the dimension of adjacent metal lines to each overlying metal line touched by a via in the first via group that is not in the second via group by at least the delta distance.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Naum B. Levin whose telephone number is 571-272-1898. The examiner can normally be reached on M-F (8:00-4:30).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Matthew S. Smith can be reached on 571-272-1907. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

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